MULTIMEDIA UNIVERSITY

STUDENT ID NO

MULTIMEDIA UNIVERSITY

FINAL EXAMINATION

TRIMESTER 1, 2017/2018

EEE1016 – ELECTRONICS 1

(All Sections / Groups)

11TH OCTOBER 2017
2:30 pm – 4:30 pm
(2 Hours)

INSTRUCTION TO STUDENTS

1. This Question paper consists of **7 pages,** including cover page and appendix, with **4 Questions** only.

2. Attempt **ALL** the questions. All questions carry equal marks and the distribution of the marks for each question is given.

3. Please w all your answers in the answer Booklet provided.

QUESTION 1

(a) An n-type *Si* semiconductor at 300° K is doped with 10^{16} phosphorus atoms cm^{-3}. Given that the electron mobility in *Si* is $\mu_n = 1350\ cm^2/V\text{-}s$ and its corresponding hole mobility is $\mu_p = 450\ cm^2/V\text{-}s$. The intrinsic carrier concentration of silicon is $n_i = 1.5 \times 10^{10}\ cm^{-3}$.

(i) Determine the majority and minority carrier concentrations in the *Si*. [4 marks]

(ii) Find the resistivity of the n-type *Si*. [2 marks]

(iii) If 10^{17} boron atoms cm^{-3} are diffused into this n-type *Si*, calculate the electron and hole concentrations. What type of semiconductor is obtained? State clearly the assumptions made in your calculation. [6 marks]

(iv) Find the drift current density in the compensated *Si* semiconductor if the applied field $E = 5$ V/cm and charge $q = 1.6 \times 10^{-19}$ C. [3 marks]

(b) Figure Q1(b) shows a diode circuit with a supply voltage, $V_S = 10$ V, and the value of the resistance, $R = 0.33\ k\Omega$.

(i) Use the piecewise-linear model to represent the *Si* diode in the circuit and sketch the equivalent circuit. [2 marks]

(ii) Determine the values of V_D and I in the circuit. Assume the Si diode has a cut-in voltage $V_\gamma = 0.7$ V and a forward diode resistance $R_f = 10\ \Omega$. [4 marks]

(iii) If the current rating of the diode is 20 mA, discuss how to limit the diode current in the circuit with additional S_i diode to a safe value for the same supply voltage and resistor. Draw your new circuit. [4 marks]

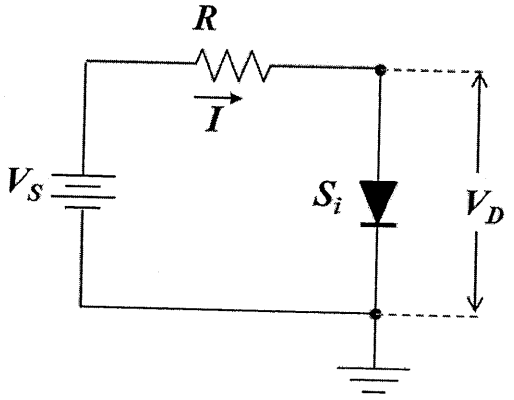

Figure Q1(b)

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QUESTION 2

(a) A DC power supply converts an AC input voltage into a constant DC output voltage. Describe the **FOUR** main stages of an AC-DC circuit, in the construction of DC power supply. [6 marks]

(b) Figure Q2(a) depicts a single-phase half-wave rectifier circuit with an input voltage waveform as shown in Figure Q2(b). Assume an ideal diode model.

(i) For the input voltage $V_i = V_m \sin \omega t$ shown in Figure Q2(b), draw its corresponding output waveform V_o, for the duration $\omega t = 0$ to $\omega t = 2.5\pi$. [3 marks]

(ii) State the expression of the average output voltage, $V_{o(av)}$, in terms of the output voltage, V_o. **PROVE** that the average (DC) output voltage $V_{o(av)}$ is approximately 31.8% of the peak input voltage V_m for the half-wave rectifier circuit. [6 marks]

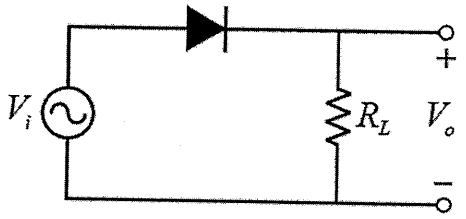

Figure Q2(a)

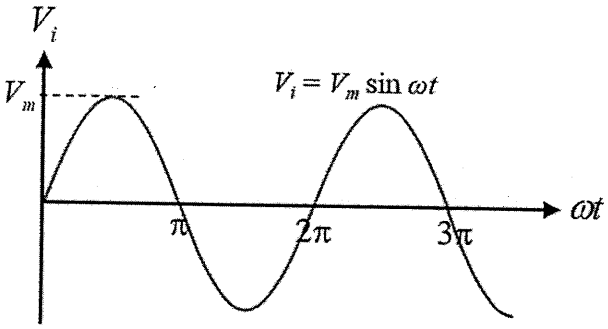

Figure Q2(b)

(c) The half-wave rectifier circuit in Figure Q2(a) has a peak input voltage $V_m = 20$ V, input frequency $f = 60$ Hz, and load resistance $R_L = 1$ kΩ. Assume the diode has a cut-in voltage, $V_\gamma = 0.7$ V, and the forward diode resistance R_f is negligible. Determine the following:

(i) Average output voltage $V_{o(av)}$, and average load current $I_{o(av)}$. [3 marks]

(ii) Root-mean-square (rms) output voltage $V_{o(rms)}$, and rms load current $I_{o(rms)}$. [3 marks]

(iii) Power absorbed by the load R_L, $P_{o(rms)}$. [2 marks]

(iv) Ripple factor of the output voltage, γ. [2 marks]

Continued ...

QUESTION 3

(a) State the biasing conditions of the base-emitter and collector-base junctions for a Bipolar Junction Transistor (BJT) to operate in the active, saturation and cut-off regions respectively. [3 marks]

(b) Sketch the transistor symbol for a pnp and a npn transistor, and then insert the flow direction for each current. [4 marks]

(c) Name three biasing configurations used in transistor amplifier circuits. Mention the biasing configuration which has a better stability and justify your answer. [4 marks]

(d) Figure Q3 shows a simple BJT amplifier biasing circuit. Given that the DC amplification factor, $\beta = 80$ and $V_{BE} = 0.7$ V. With the given current and voltages, determine the values of R_C, R_E and R_B. [7 marks]

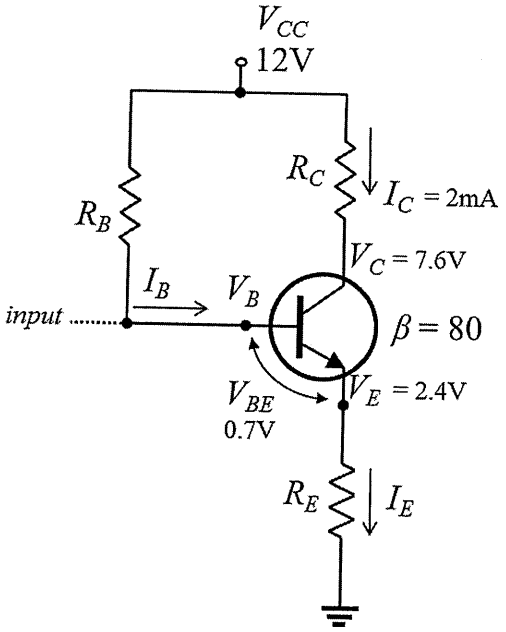

Figure Q3

(e) Due to temperature increase, the amplification factor, β, of Figure Q3 is increased by 10%. Using the resistors values obtained from Question 3 (d), calculate the new values of I_C, V_C , V_E and V_{CE}. [7 marks]

Continued ...

QUESTION 4

(a) Figure Q4(a) shows a two-port circuit, connected to a signal source, $v_s = 5\text{mV}_{\text{rms}}$ and a source resistance, $R_S = 200\Omega$. The output of the circuit is connected to a load, $R_L = 1.2\text{k}\Omega$. The two-port circuit has the following characteristics:

Table Q4(a)

No-load voltage gain, Av_{NL}	200
Input voltage, v_{in}	$3.75\text{mV}_{\text{rms}}$
Output voltage, v_{out}	$-150\text{mV}_{\text{rms}}$

(i) Draw the equivalent circuit of the two-port system. [3 marks]
(ii) Calculate the internal impedance Z_{in} of the two-port circuit. [3 marks]
(iii) Calculate the output impedance Z_{out} of the two-port circuit. [4 marks]

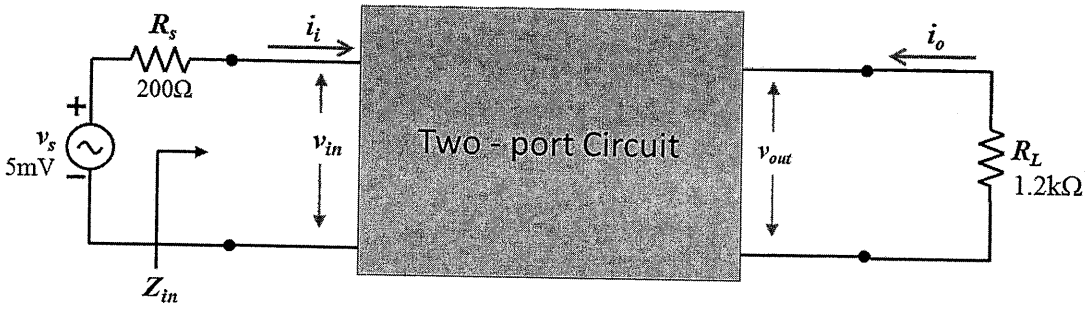

Figure Q4(a): A Two-Port Circuit

(b) Figure Q4(b) is a single stage BJT amplifier circuit. Draw the r_e model of the small signal equivalent circuit of the amplifier by showing all external and parametric components of the transistor. [3 marks]

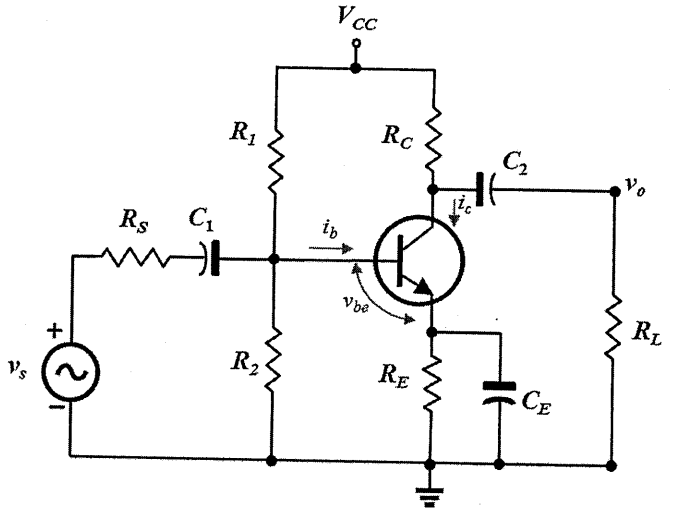

Figure Q4(b): A Single Stage BJT Amplifier

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(c) Figure Q4(c) shows a BJT transistor amplifier circuit with $\beta = 100$.

(i) Determine whether or not approximation method can be used to determine the DC voltage V_B and hence calculate V_E. [4 marks]

(ii) Determine the emitter current I_E and calculate the internal emitter resistance r_e of the BJT. [3 marks]

(iii) Draw the r_e model of the amplifier circuit and show all the known values of its components, given that the output resistance, $r_o = \infty$ [2 marks]

(iv) Calculate the input impedance Z_{in} and the effective input impedance Z'_{in} seen from the signal generator. [3 marks]

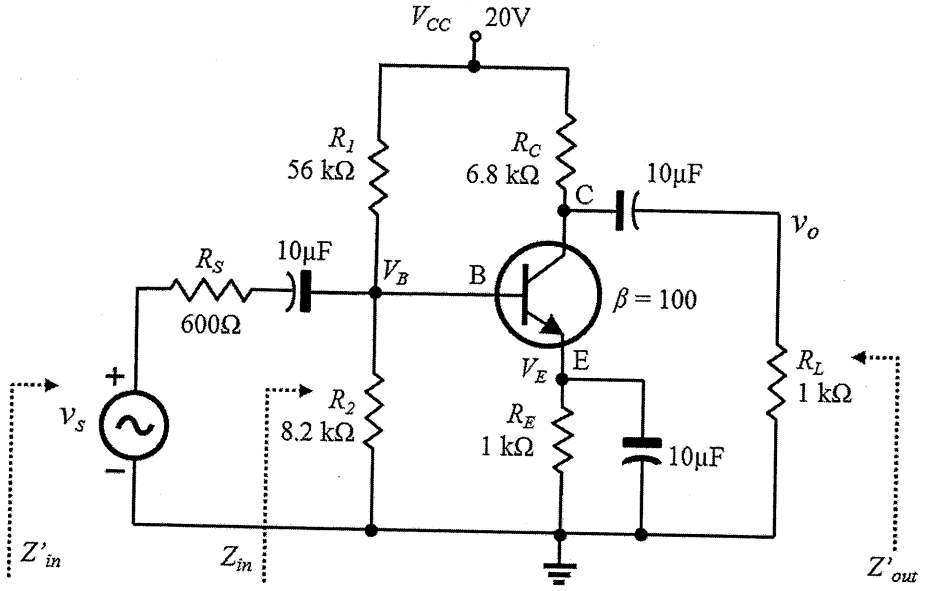

Figure Q4(c)

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Appendix

1. Charge of electron, $q = 1.6 \times 10^{-19}$ coulomb
2. Mass of electron, $m = 9.11 \times 10^{-31}$ kg
3. Holes and electrons in pure semiconductor, $p = n = n_i$
4. Law of Mass-action, $np = n_i$
5. Law of Electrical Neutrality, $\left(N_D^+ + p\right) = \left(N_A^- + n\right)$

   When all imprurities are ionised, $\left(N_D + p\right) = \left(N_A + n\right)$
6. In *n-type* semiconductor, $n_n \approx N_D$. In *p-type* semiconductor, $p_p \approx N_A$
7. Drift current density, $J_{drift} = J_n + J_p = \left(n\mu_n + n\mu_p\right)qE = \sigma E$
8. Characteristics of common semiconductors

Semiconductor	Intrinsic carriers/cm^3	μ_n (cm^2/V-s)	μ_p (cm^2/V-s)
GaAs	1.7×10^6	8500	400
Si	1.5×10^{10}	1350	410
Ge	2.5×10^{13}	3800	1800

9. Shockley diode equation, $i = I_o\left(e^{\left(\frac{V}{\eta V_T}\right)} - 1\right)$ where $V_T = \dfrac{kT}{q} = 26\text{mV}$
10. Form factor of rectifier, $FF = \dfrac{V_{o(rms)}}{V_{o(av)}}$
11. Ripple factor of rectifier, $\gamma = \sqrt{\left(\dfrac{V_{o(rms)}}{V_{o(av)}}\right)^2 - 1} = \sqrt{FF^2 - 1}$
12. RMS output voltage of half-wave rectifier, $V_{o(rms)} = \dfrac{V_m}{2}$
13. RMS output voltage of full-wave rectifier, $V_{o(rms)} = \dfrac{V_m}{\sqrt{2}}$
14. Average output voltage of half-wave rectifier, $V_{o(dc)} = \dfrac{V_m}{\pi}$
15. Average output voltage of full-wave rectifier, $V_{o(dc)} = \dfrac{2V_m}{\pi}$
16. Current flows in BJT, $I_C = \beta I_B$ and $I_E = \left(\beta + 1\right)I_B$
17. Internal emitter resistance of BJT, $r_e = \dfrac{V_T}{I_E} = \dfrac{26\text{mV}}{I_E}$